## REMARKS/DISCUSSION OF ISSUES

***Claim Summary***

By this Amendment, claims 1 and 11 have been canceled, without prejudice and without disclaimer of the subject matter, and claims 2-10 and 12-15 have been amended to correct informalities in the claim language and to more clearly define the invention. Further, independent claims 16-18 have been submitted for the Examiner's consideration, where claims 16 and 17 include subject matter of canceled claims 1 and 11, respectively.

Claims 2-10 and 12-18 are pending in the application. Applicants respectfully submit that all pending claims are in condition for allowance.

***35 U.S.C. § 112 Rejection - Claims 1-15***

The Office Action of January 15, 2008, rejects claims 1-15 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. In particular, the Examiner referenced claims 1 and 11 reciting local control device (36) and local control devices (36).

Claims 1 and 11 have been canceled, and newly submitted claims 16-18 do not recite the claim language to which the Examiner objected. Accordingly, Applicants submit that the rejection is now moot, and respectfully request withdrawal of the rejection under 35 U.S.C. § 112, second paragraph.

***35 U.S.C. § 102 Rejection - Claims 1-15***

The Office Action of January 15, 2008, rejects claims 1-15 under 35 U.S.C. § 102(e) as being anticipated by CHANDRAKASAN et al. (U.S. Patent Publication Application No. 2004/0183588). Applicants respectfully traverse the rejection because CHANDRAKASAN et al. does not disclose each and every element of the claims.

Applicants rely at least on the following standards with regard to proper rejections under 35 U.S.C. § 102. Notably, anticipation requires that each and every element of the claimed invention be disclosed in a single prior art reference. *See, e.g., In re Paulsen,* 30 F.3d 1475, 31 USPQ2d 1671 (Fed. Cir. 1994); *In re Spada,* 911 F.2d 705, 15 USPQ2d 1655 (Fed.

Cir. 1990); *W.L. Gore & Assoc., Inc. v. Garlock, Inc.,* 721 F.2d 1540, 220 USPQ 303, 313 (Fed. Cir. 1983). Alternatively, anticipation requires that each and every element of the claimed invention be embodied in a single prior art device or practice. *See, e.g., Minnesota Min. & Mfg. Co. v. Johnson & Johnson Orthopaedics, Inc.,* 976 F.2d 1559, 24 USPQ2d 1321 (Fed. Cir. 1992). For anticipation, there must be no difference between the claimed invention and the reference disclosure, as viewed by a person of ordinary skill in the field of the invention. *See, e.g., Scripps Clinic & Res. Found. v. Genentech, Inc.,* 927 F.2d 1565, 18 USPQ2d 1001 (Fed. Cir. 1991).

Applicants' silence on certain aspects of the rejection is by no means a concession as to their propriety. Rather, because the applied art fails to disclose at least one feature of the claims, for at least the reasons discussed below, Applicants respectfully submit that the rejection is improper and should be withdrawn.

Claim 1 (claim 16)

Independent claim 1 has been canceled, and replaced by independent claim 16, which recites, in part:

" *... a global monitor configured to monitor at least one working parameter related to a working condition of the integrated circuit, wherein each of the first and second computation islands comprises a local controller for independently tuning the corresponding at least one utility value based on the monitored at least one working parameter, the local controller communicating with a global controller to obtain a pre-set level of performance of the integrated circuit.*"

CHANDRAKASAN et al. does not teach or suggest at least these features. CHANDRAKASAN et al. is directed to PMOS and NMOS transistors formed on a CMOS triple well transistor structure. The Examiner apparently asserts that the first and second computation islands are disclosed by the PMOS and NMOS transistors. *See* Office Action, p. 3 (referring to paragraphs [0012], [0022]-[0023], [0043], [0047] of CHANDRAKASAN et al.). The PMOS and NMOS transistors may be individually tuned by respectively applying bias voltages Vbp and Vpn to the n-type well 123 of the PMOS transistor and the p-type well

124 of the NMOS transistor, provided by a single dual open loop controller 70. *See, e.g.,* paragraphs [0059]-[0060], [0070].

The Office Action asserts that this controller 70 discloses three elements of claim 1: a global monitor, a global controller and a local controller. *See* Office Action, p. 4. However, the controller 70 cannot teach a local controller because, as recited in claim 16, each of the first and second computation islands includes a local controller for independently tuning the at least one utility value. In other words, each computation island has a local controller, while CHANDRAKASAN et al. teaches one controller 70 for controlling (at least) two transistors, which the Examiner equates to computation islands.

Accordingly, for at least the reasons stated above, Applicants respectfully submit that claim 16 is allowable.

Claim 11 (claim 17)

Independent claim 11 has been canceled, and replaced by independent claim 17, which recites, in part:

" *... each of the computation islands comprising a local controller for independently tuning the at least one utility value for the computation island, the method comprising: ... independently tuning the at least one utility value for at least one computation island of the plurality of computation islands using the corresponding local controller, based on the monitored at least one working parameter; and controlling each local controller of each computation island using a global controller to obtain a pre-set level of performance of the integrated circuit.*"

CHANDRAKASAN et al. does not teach or suggest at least these features. As stated above with respect to claim 16, the Office Action asserts that the controller 70 discloses a global controller and a local controller. *See* Office Action, pp. 4, 5. However, the controller 70 cannot teach a local controller because, as recited in claim 17, each of the computation islands includes a local controller for independently tuning the at least one utility value. In other words, each computation island has a local controller, while CHANDRAKASAN et al.

teaches one controller 70 for controlling (at least) two transistors, which the Examiner equates to computation islands.

Accordingly, for at least the reasons stated above, Applicants respectfully submit that claim 17 is allowable.

Claims 2-10 and 12-15

With regard to claims 2-10 and 12-15, Applicants assert that they are allowable at least because they depend, directly or indirectly, from independent claims 16 and 17, respectively, which Applicants submit have been shown to be allowable, as well as in view of their additional recitations. Accordingly, Applicants respectfully request withdrawal of the rejection of claims 2-10 and 12-15 under 35 U.S.C. § 102(b).

***Claim 18***

Newly submitted independent claim 18 is allowable at least for substantially the same reasons discussed above with respect to claims 16 and 17.

Further, claim 18 recites an interface island for interfacing first and second computation islands. The Examiner asserts (in addressing original claim 7) that an interface island is taught by paragraphs [0016], [0022]-[0023], [0060] of CHANDRAKASAN et al. *See* Office Action, p. 4. These portions of CHANDRAKASAN et al. generally describe PMOS and NMOS transistors formed in a triple-well structure. However, there is no teaching or suggestion of an interface island. In fact, to the extent that the Examiner is asserting that the PMOS and NMOS transistors disclose first and second computation islands, there is no disclosure of additional component(s) teaching the interface island for interfacing the PMOS and NMOS transistors.

Accordingly, for at least the reasons stated above, Applicants respectfully submit that claim 18 is allowable.

## CONCLUSION

In view of the foregoing explanations, Applicants respectfully request that the

Examiner reconsider and reexamine the present application, allow claims 2-10 and 12-18 and pass the application to issue. In the event that there are any outstanding matters remaining in the present application, the Examiner is invited to contact Van C. Ernest (Reg. No. 44,099) at (571) 283.0720 to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment (except for the issue fee) to Deposit Account No. 50-0238 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17, particularly extension of time fees.

Respectfully submitted on behalf of:

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